REMARKS

The present Amendment amends claims 6, 14 and 27 and leaves claims 1-5, 7-17, 15, 16, 18-26, 28-31, 36-39, 41 and 42 unchanged. Therefore, the present application has pending claims 1-16, 18-31, 36-39, 41 and 42.

Applicants acknowledge the Examiner's indication in paragraph 6 of the Office Action that claims 6, 7 and 31 are allowed.

In the outstanding Office Action, the Examiner rejected claims 1-5, 8-16, 18-30, 38 and 39 under 35 USC §102(b) as being anticipated by Ninomiya (U.S. Patent No. 5,819,054); and rejected claims 36, 37, 41 and 42 under 35 USC §103(a) as being unpatentable over Ninomiya. These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1-5, 8-16, 18-30, 36-39, 41 and 42 are not taught or suggested by Ninomiya whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to each of the claims so as to more clearly recite that according to the present invention a first cable is used to make a connection between an access path interface unit in the channel interface package and an access path interface unit in the memory package and a second cable different from the first cable is used to make a connection between an access path interface unit in the disk interface package and an access path interface unit in the memory package. Thus, according to the present invention, in disk array controller the plurality of channel interface packages are connected to the plurality of memory packages via

first cables and the plurality of disk interface packages are connected to the plurality of memory packages via second cables different from the first cables. Such features are clearly not taught or suggested by any of the references of record particularly Ninomiya whether taken individually or in combination with each other.

Ninomiya discloses a disk array system which includes a plurality of host adaptors 1, a plurality of disk adaptors 2, a plurality of cache memory units 3, and a plurality of disks 5. As taught in Ninomiya, in the disk array system, the plurality of host adaptors 1 are connected to the plurality of cache memory units 3 via bus 4 and the plurality of disk adaptors 2 are connected to the plurality of cache memory units 3 also via the bus 4. In the Office Action the Examiner incorrectly alleges that a bus and a cable are the same. However, the bus identified by the Examiner in Ninomiya is not equivalent to a cable for various reasons as would be known to those of ordinary skill in the art.

In Ninomiya, the bus is printed on a back plane as a printed circuit and the plurality of host adaptors, the plurality disk adaptors and the plurality cache memory units are connected to the back plane. The Examiner's attention is directed to col. 8, lines 3-15 and Fig. 7 of Ninomiya. Thus, in Ninomiya if a part of the bus printed on the back plane becomes broken or defective, all units of the disk array system including the host and disk adaptors and cache memory units that are themselves attached to the back plane must be replaced. Such is the not case in the present invention since cables are used.

In the present invention, if one or more of the cables is broken, only the broken cable need to be replaced thereby not affecting the other cables or the

elements connected to the cable or elements connected to other cables. Thus, it is quite clear that the cables recited in the claims of the present application are entirely different from the bus as taught by Ninomiya.

Further, due to use of the cables according to the present invention the layout of the parts of the disk array controller as recited in the claims of the present application is infinitely reconfigurable (movable) as needed. Such reconfigurable (moveable) layout is not possible in Ninomiya. As is quite clear from the above, Ninomiya has a fixed layout since the bus is part of the back plane. As per Ninomiya, the host adaptors, disk adaptors and cache memory unit are themselves attached to the back plane in a fixed configuration. Thus, the layout of the bus, the host adaptors, disk adaptors and cache memory as taught by Ninomiya is fixed and as such is not movable. The present invention allows for a flexible layout since cables are being used thereby eliminating any complicated structures or allowing the system to be reconfigured and scaled up or down as necessary. Such is clearly not possible in Ninomiya.

Accordingly, Ninomiya fails to teach or suggest that connections are made between the access path interface units in the channel interface package and the access path interface units in the memory package by first cables and between the access path interface in the disk interface unit package and the access path interface unit in the memory package by second cables different from the first cables as now recited in the claims.

Further, according to the present invention, it appears that claims 13-16, 18-30, 36-39, 41 and 42 recite many of the same features recited in claims 6, 7 and 31

determined by the Examiner to be allowed over the prior art of record. In fact, many of these claims appear to recite features more narrower than that recited in claims 6, 7 and 31.

Thus, for example, claim 13 recites a disk array controller similar to claim 6 having a channel interface unit, a disk interface unit, a memory interface unit, an interface platter, a memory platter, plural cables and a selector unit whereas claim 6 recites a channel interface package, a disk interface package, a memory package and a platter. The difference is that claim 13 recites additional features such as the interface platter and the selector unit. In addition, claim 13 recites that a path is provided so as to couple the channel interface unit to the first cable and such path is printed on the interface platter, that a further path couples the disk interface unit to the second cable and such further path is printed on the interface platter, and that a still further path couples the memory unit to the third cable different from the first and second cables and that the still further path is printed on the memory platter.

There is no teaching or suggestion in Ninomiya of the above described differences between claims 13-16, 18-30, 36-39, 41 and 42 and claims 6, 7, and 13.

Therefore, as is quite clear from the above example, claims 13-16, 18-30, 36-39, 41 and 42 recite similar features as claims 6, 7 and 31 and the additional features recited in claims 13-16, 18-30, 36-39, 41 and 42 make these claims more narrower than claims 6, 7 and 31. Accordingly, Applicants submit that claims 13-16, 18-30, 36-39, 41 and 42 should be allowable for at least the same reasons used by the Examiner to determine that claims 6, 7 and 31 are allowed over the prior art of record including Ninomya..

As is clear from the above, the features of the present invention now more clearly recited in the claims are not taught or suggested by Ninomiya whether taken individually or in combination with any of the other references of record. Therefore, reconsideration and withdrawal of the 35 use §102(b) rejection of claims 1-5,8-16, 18-30,38 and 39 as being anticipated by Ninomiya and the 35 use §103(a) rejection of claims 36,37,41 and 42 as being unpatentable over Ninomiya are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-5, 8-16, 18-30, 36-39, 41 and 42. In view of the foregoing amendments and remarks, Applicants submit that claims 1-16, 18-31, 36-39, 41 and 42 are in condition for allowance. Accordingly, early allowance of claims 1-16, 18-31, 36-39, 41 and 42 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (501.39293X00).

Respectfully submitted,

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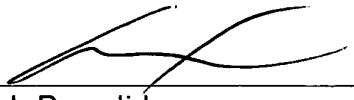

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